A General Partition Scheme for Gate Leakage Current Suitable for MOSFET Compact Models

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Abstract

For the first time, it is rigorously shown that the source/drain partition of gate leakage current in a MOSFET is identical to that of inversion charge. This paper provides model developers a general recipe in addressing the partition issue and enables more consistent model parameter extraction methodology for MOSFETs in the sub-100nm technology.

Introduction

As gate leakage current density continues to increase for every process generation, accurate compact models for I_G and source/drain partition of I_G are extremely critical to validate circuit performance in the sub-100nm technology. From characterization standpoint, these models further enable accurate extraction of I_{DS} from I_D, thus allowing more accurate extraction of important compact-model parameters such as mobility and saturation velocity. Previously, the partition issue was addressed in the weak-tunneling regime by Cao et al. in BSIM4 [1], where the change in surface potential due to gate leakage was treated as a perturbation. Despite the model simplicity, it is unclear how I_G is partitioned beyond the weak tunneling regime, where the effect of surface-potential change on the leakage current density cannot be ignored. Moreover, the partition expression is applicable only to the specific underlying leakage model previously developed by the authors [2]. No guidance was provided on how to handle more complicated leakage expressions that one would possibly encounter when modeling the tunneling through high-k or stacked gate dielectric.

In this paper we address above issues by uncovering the underlying principle that governs the partition of gate current. We show that, to a good approximation, the gate current partition rule is identical to the standard inversion charge partition rule [3]. The derivation of the partition scheme does not assume any specific functional dependence of leakage-current density on the local surface potential, nor does its validity rely on the weak tunneling assumption. The conclusions of this study are therefore applicable to general MOSFET compact models. In fact, it can be shown that the BSIM4 partition model is simply the outcome of this partition scheme when applied to the 1-D leakage model presented in [2].

Model derivation

Our main objective is to obtain a formal solution to the continuity equation for the channel current in the presence of gate leakage. Under drift-diffusion approximation, the channel current I(y) and its continuity equation can be written as follows:

$$I(y) = \mu C_{ox} U \frac{d\varphi_s}{dy} \tag{1}$$

$$\frac{\mu C_{ox}}{2\alpha} \frac{d^2 U^2}{dy^2} = J_G \tag{2}$$

where

$U \equiv V_{GS} - V_{TH} - \alpha(\varphi_s - \varphi_{ss})$
$y \equiv$ Distance from source along the channel
$\varphi_s \equiv$ Surface potential
$\varphi_{ss} \equiv \varphi_s$ at source end of the channel
$V_{TH} \equiv$ Threshold voltage
$\alpha \equiv$ Body factor
$\mu \equiv$ Mobility
$J_G \equiv$ Leakage current density

As there exist infinite sets of (I_{GS}, I_{GD}, I_{DS}) to yield the measured terminal currents (I_S, I_D, I_G), we *Define* I_{DS} as the channel current in the absence of gate leakage, leaving no ambiguity in determining I_{GD} and I_{GS}, as shown in Figure 1. The I_{DS} thus defined satisfies the following continuity equation commonly seen in the compact-model literature:

$$I_{DS} = \mu C_{ox} U_0 \frac{d\varphi_{s0}}{dy} \tag{3}$$

$$-\frac{\mu C_{ox}}{2\alpha} \frac{d^2 U_0^{\,2}}{dy^2} = 0 \ , \tag{4}$$

where U_0, φ_{s0}, and φ_{ss0} are the leakage-free counterparts of U, φ_s and φ_{ss}, respectively.

Due to the gate leakage, the channel current I(y) deviates from I_{DS} and is no longer a constant along the channel. Corresponding change in the surface potential is needed to support the change in current. These changes are fully comprehended in the change of U^2. Eq.(2) is a linear second-order differential equation in U^2 with a source term J_G. Its solution consists of a homogeneous component U_0^2 and a correction term $U_1^2 \equiv U^2 - U_0^2$. As U_0^2 is known from solving Eq.(5), U_1^2 can be formally solved using simple Green's function technique. The Green's function we are seeking has to satisfy the following condition:

$$\frac{\mu C_{ox}}{2\alpha} \frac{d^2 G(y, y_0)}{dy^2} = \delta(y - y_0), \qquad G(0, y_0) = G(L, y_0) = 0 \tag{5}$$

which leads to the solution:

$$G(y, y_0) = \begin{cases} \dfrac{2\alpha}{\mu C_{ox}}(y_0 / L - 1)y, \; y < y_0 \\ \dfrac{2\alpha}{\mu C_{ox}}(y / L - 1)y_0, \; y_0 < y \end{cases} \qquad (6)$$

The inhomogeneous part of U^2 is therefore:

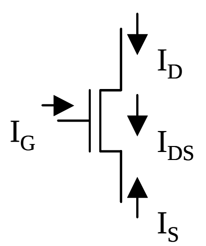
$$U_1(y)^2 = \int_0^L G(y, y_0) J_G(y_0) dy_0 \qquad (7)$$

Combing Eq.s (1), (3), and (7) gives I_S and I_{GS}:

$$I_S = \frac{\mu C_{ox}}{2\alpha} \left. \frac{dU^2}{dy} \right|_{y=0} = -I_{DS} + \int_0^L (1 - y_0 / L) J_G(y_0) dy_0$$

$$I_{GS} = \int_0^L (1 - y_0 / L) J_G(y_0) dy_0 \qquad (8)$$

Note that in arriving at Eq.(8), no special assumption has been made regarding either the strength or the functional form of J_G. Hence, Eq.(2) holds even if leakage introduces significant channel de-biasing, and is expected to be general for all different model formulation. Note also that the mobility is assumed to be constant throughout the derivation. The error resulting from this assumption will be examined in the following section.



$$I_{GS} \equiv -I_S - I_{DS}$$

$$I_{GD} \equiv I_{DS} - I_D$$

Figure 1: Sign convention for various current components. Defining I_{DS} as the drain current in the absence of gate leakage allows I_{GS} and I_{GD} to be uniquely determined in both the compact model derivation and the numerical validation.

Numerical validation

In order to verify the partition scheme, the current continuity equation in Eq.(2) is numerically solved, including mobility degradation and velocity saturation so that the error due to the constant-mobility assumption can be examined. Handling velocity saturation near the drain requires the knowledge of V_{DSAT} in order to provide the voltage boundary condition for the continuity equation. In the absence of gate leakage, V_{DSAT} defined under common compact-modeling approach can be analytically calculated. With the gate leakage turned on, however, the original current boundary condition that defines V_{DSAT} is numerically solved together with the continuity equation in order to ensure the numerical robustness. The total leakage current I_G is calculated either self-consistently (SC) with the channel current or in a post-processing, non-self-consistent (NSC) manner. The NSC solution provides the I_{DS} in the absence of leakage, and the SC solution provides the I_S and I_D needed to complete the extraction of I_{GS} and I_{GD}. On the other hand, in both the SC and NSC solutions, the partition integral on the right-hand side of Eq,(8) is also computed. The comparison between the I_{GS} calculated using the partition integral, hereafter referred to as *modeled* I_{GS}, and the I_{GS} extracted from simulated I_S and I_{DS}, hereafter referred to as *extracted* I_{GS}, provides sufficient evidence to validate the partition scheme.

Figure 2 shows typical I-V characteristics obtained with the numerical solver in a 2μm long device. All parameters used in the model correspond to the devices published in [4] except that, for the sole purpose of model validation, the 1-D leakage model parameters are tweaked to produce high leakage of about 1 kA/cm^2 at V_{GS}=1.2 V. Apparently, high leakage current causes the net current to flow out of the drain at high gate bias. Figure 3 shows the comparison between the modeled I_{GS} with the extracted I_{GS}. The close agreement validates the partition model.

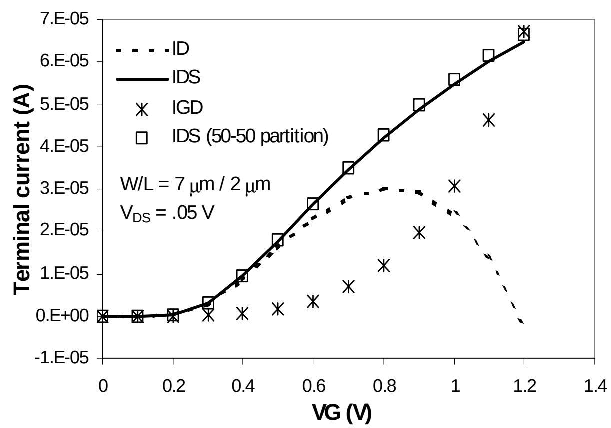


Figure 2: Typical I-V characteristics in a 2μm long device at V_{DS} = 0.05 V obtained from the numerical continuity equation solver. I_D (dashed line) is obtained with the SC solution, I_{DS} (solid line) with the NSC solution, and the extracted I_{GD} obtained from $I_{DS} - I_D$. Also shown is the I_{DS} extracted from the SC I_G and I_D, assuming a 50-50 source/drain partition for I_G (squares).

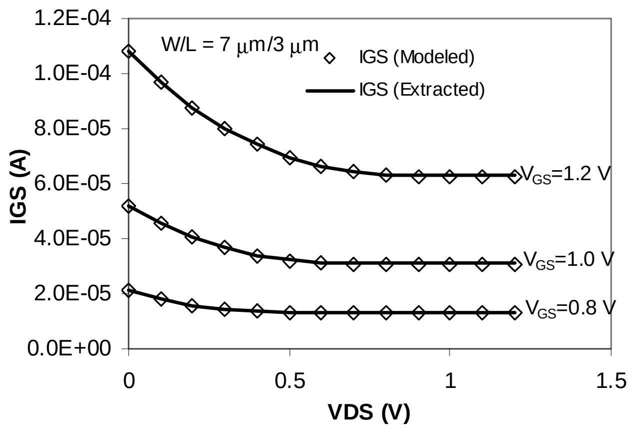


Figure 3: Good agreement is observed between the modeled I_{GS} and the extracted I_{GS}, verifying the partition scheme.

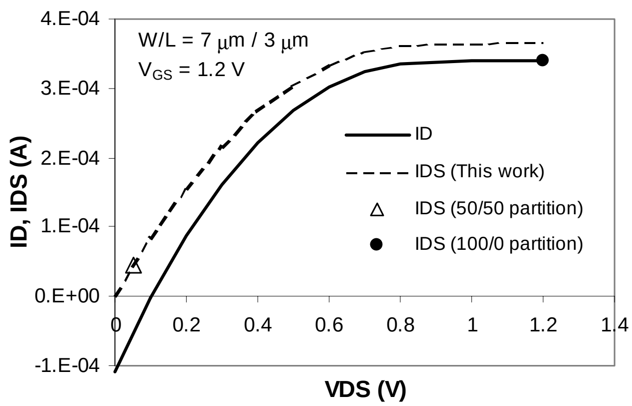


Figure 4: I_D and I_{DS} corrected for gate leakage. Simple correction method which assumes that all I_G goes into the source at high V_{DS} yields appreciable error in extracting saturation I_{DS}.

An immediate benefit of the accurate partition model can be seen in I_{DS} extraction needed for compact-model calibration. When extracting I_{DS} from terminal current measurement, it is a common practice to assume that I_G is equally divided between source and drain (50/50 partition) at low V_{DS} and that all I_G enters source (100/0 partition) at high V_{DS}. For the bias condition and device shown in Figure 2, such assumption leads to about 3% error in the extracted I_{DS}. The error grows quickly as channel length increases, especially for devices operating in saturation. In a 3µm device shown in Figure 4, an error of about 10% is observed in the saturation I_{DS} obtained with the simple 100/0 partition. The 100/0 partition always tends to underestimate I_{DS} due to ignoring the I_{GD} contribution in I_D.

To further validate the general partition scheme beyond the weak tunneling regime, devices that exhibit strong channel de-biasing effects have been simulated with the numerical model. For the level of leakage current density chosen, devices with channel length greater than about 4µm show significant leakage-current reduction due to the channel de-biasing. An example is shown in Figure 5, where the I_G obtained from the SC calculation is more than 30% lower than that from the NSC calculation. The large I_G reduction is readily explained by inspecting the surface potential along the channel (Figure 6). As large I_G enters source and drain through the channel, the voltage drop across the resistive channel forces the surface potential near the middle of the channel to become higher than that near the source and drain, causing a considerable reduction in local oxide field and J_G.

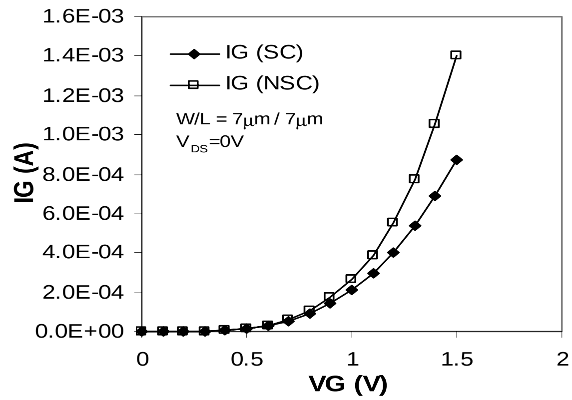


Figure 5: I_{GS} obtained with the numerical 1-D continuity equation solver in a 7µm/7µm device. Results from the self-consistent solution are compared to those with the non-self-consistent solution. The difference between SC and NSC is explained in Fig.6.

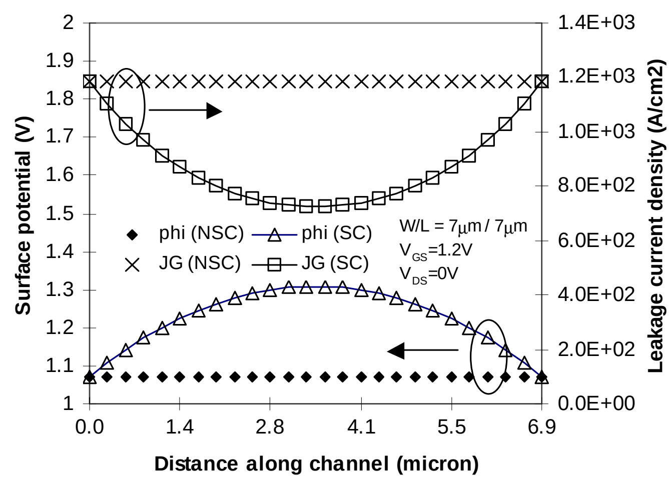


Figure 6: Surface potential (phi) and leakage current density (J_G) along the channel obtained with SC and NSC solutions explain the pronounced reduction in I_G due to channel debiasing.

In spite of the significant channel de-biasing, the partition scheme is shown in Figure 7 to remain valid, judging from the good agreement between the extracted I_{GS} and the modeled I_{GS} based on the SC surface potential. Note that a large difference exists between the modeled I_{GS} based on the NSC surface potential and the extracted I_{GS}. Such

difference is mainly attributed to the channel de-biasing rather than the inaccuracy of the partition scheme.

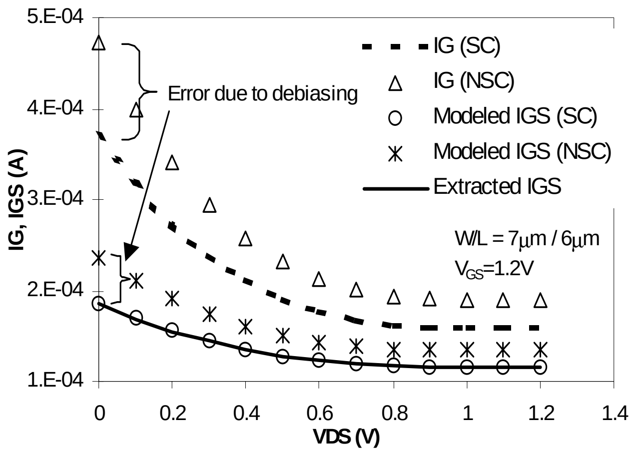


Figure 7: SC vs. NSC I_G and I_{GS}. Modeled I_{GS} obtained with the SC and NSC surface potentials (circles and stars) are compared to the extracted I_{GS}, I_{GS}. De-biasing results in error in NSC I_G and I_{GS}, however, the partition scheme remains valid.

As the partition scheme is derived based on the constant-mobility assumption, error becomes more pronounced in short devices. Figure 8 shows the comparison between the extracted I_{GS} and the modeled I_{GS} in a .12 μm device. The partition scheme is observed to underestimate I_{GS}. This is expected as the partition scheme has essentially over-estimated the mobility on the drain side of the channel, thus assigning more I_G to the drain than realistic. Further inspection of the mobility and leakage current density in Figure 9 provides more insight into the source of the error. Not only is the mobility variation along the channel larger in the short device, the (normalized) leakage current density near the drain is higher in the short device because of the lower V_{DS} required to reach saturation. However, the impact of this error on I_{DS} extraction is negligible since I_D is several orders of magnitude higher than I_G in short devices.

Conclusion

For the first time, a general gate-current partition scheme has been derived and numerically validated. It is found that the gate current is partitioned the same way that the inversion charge is partitioned. The partition scheme has been validated with the numerical solutions of the current continuity equation in both weak and strong tunneling regimes. In long-channel devices under saturation, correct I_G partition is found to have considerable impact on the extracted saturation I_{DS}. The partition scheme provides compact model developers with a general recipe in attacking this issue and enables more consistent model parameter extraction methodology for MOSFETS in sub-100nm technology.

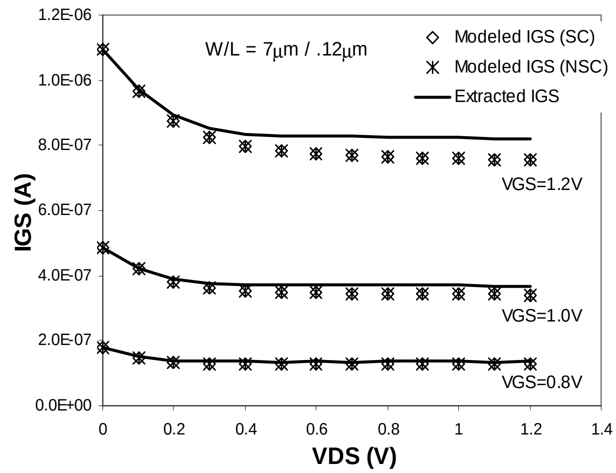


Figure 8: I_{GS} in short device with effective channel length .12 μm. The partition integral Eq.(8), used to calculate the modeled I_{GS} (SC) and I_{GS} (NSC), yields about 10% error in the saturation region compared to the extracted I_{GS}. Meanwhile, Channel de-biasing effect is negligible.

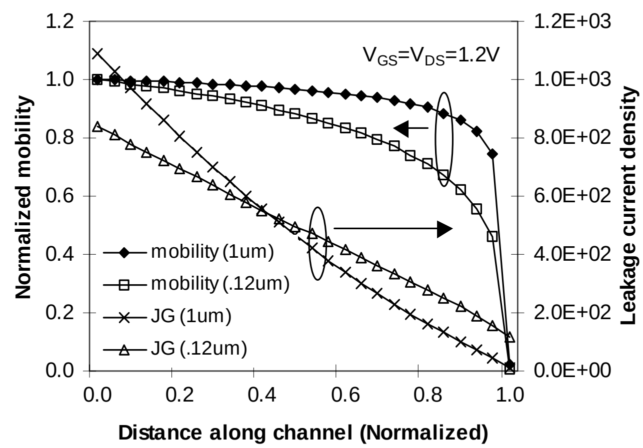


Figure 9: Normalized mobility and leakage current density along the channel in devices with effective channel length of 1μm and .12μm. The larger error in the partition integral for short devices is due to both the larger variation of mobility and relatively more significant contribution to I_G from near the drain side of the channel.

References

[1] Cao el al., "BSIM4 gate leakage model including source-drain partition," IEDM Tech. Dig. p.815, 2000.

[2] W.-C. Lee and C. Hu, "Modeling gate and substrate currents due to conduction- and valence-band electron and hole tunneling,", Symp. On VLIS Tech., p.198, 2000.

[3] D. Ward and R. Duton, "A charge-oriented model for MOS transistor capacitances," IEEE J. Solid-State Ckts., vol.SC-13, p.703, 1978.

[4] Y. P. Tsividis, "Operation and Modeling of the MOS transistor, 2nd ed." New York, McGraw-Hill, 1999

[5] S. Tyagi, et al., "A 130nm genheration logic technology Featuring 70nm transistors, dual Vt transistors and 6 layers of Cu interconnects," IEDM Tech. Dig., p. 567, 2000